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PHAc: Posit Hardware Accelerator for Efficient Arithmetic Operations

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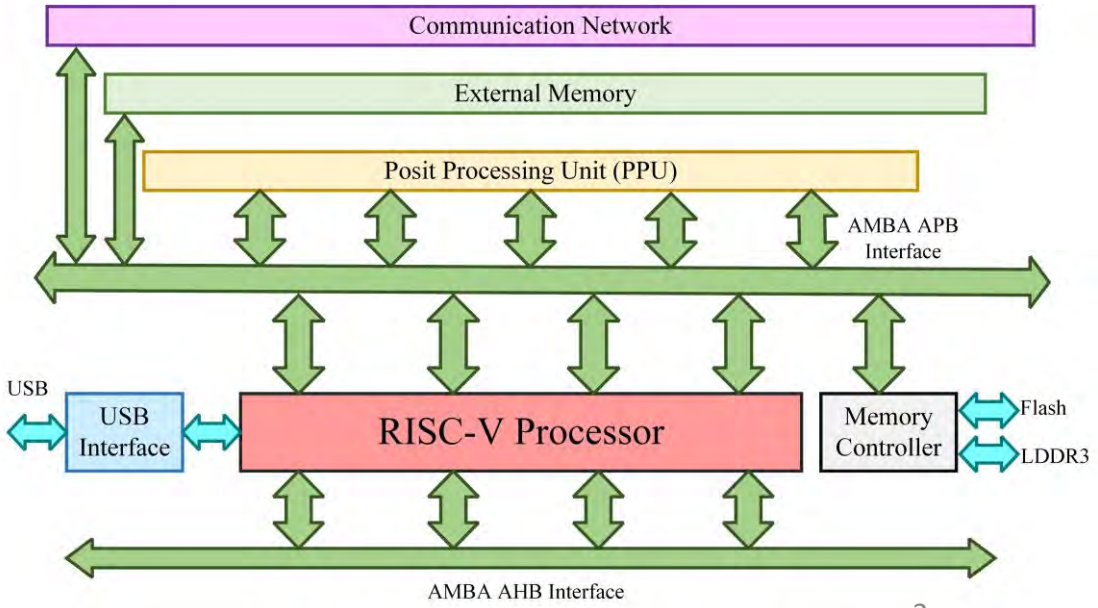
Outline

- Motivation for the Work
- Introduction
- Architectures for Posit Adder/Subtractor and Multiplier
- Control Unit
- Implementation Results on FPGA
- Conclusion
- References

Motivation for the Work

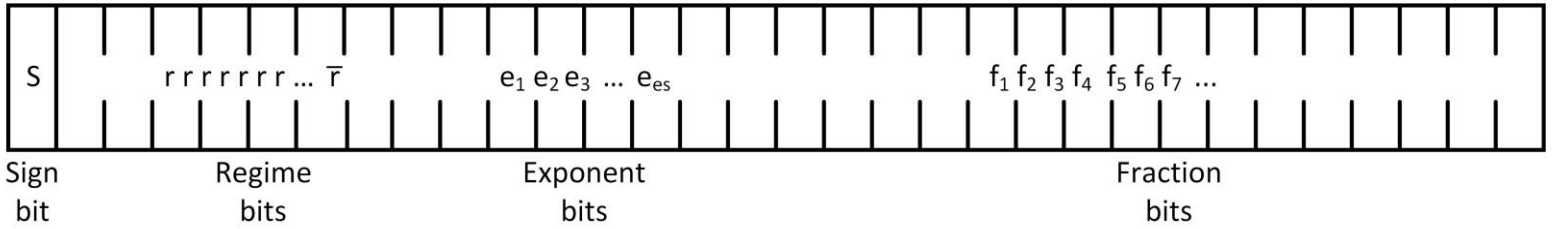
- Sufficiently accurate and low-cost arithmetic is needed
- IoT/Embedded systems have limited power and area budgets
  - With demand for high performance
- Alternatives of IEEE-754[KAHA96] compliant arithmetic
  - Anchored numbers from ARM, Posit, bfloat16, etc.
- Posit[GUST17]
  - Quick, better dynamic ranges
  - Direct drop-in replacement for IEEE-754
    - Can replace FPUs in SoCs



[KAHA96] Kahan, William. "IEEE standard 754 for binary floating-point arithmetic." Lecture Notes on the Status of IEEE 754.94720-1776 (1996): 11.
[GUST17] Gustafson, John L., and Isaac T. Yonemoto. "Beating floating point at its own game: Posit arithmetic." *Supercomputing Frontiers and Innovations* 4.2 (2017): 71-86.

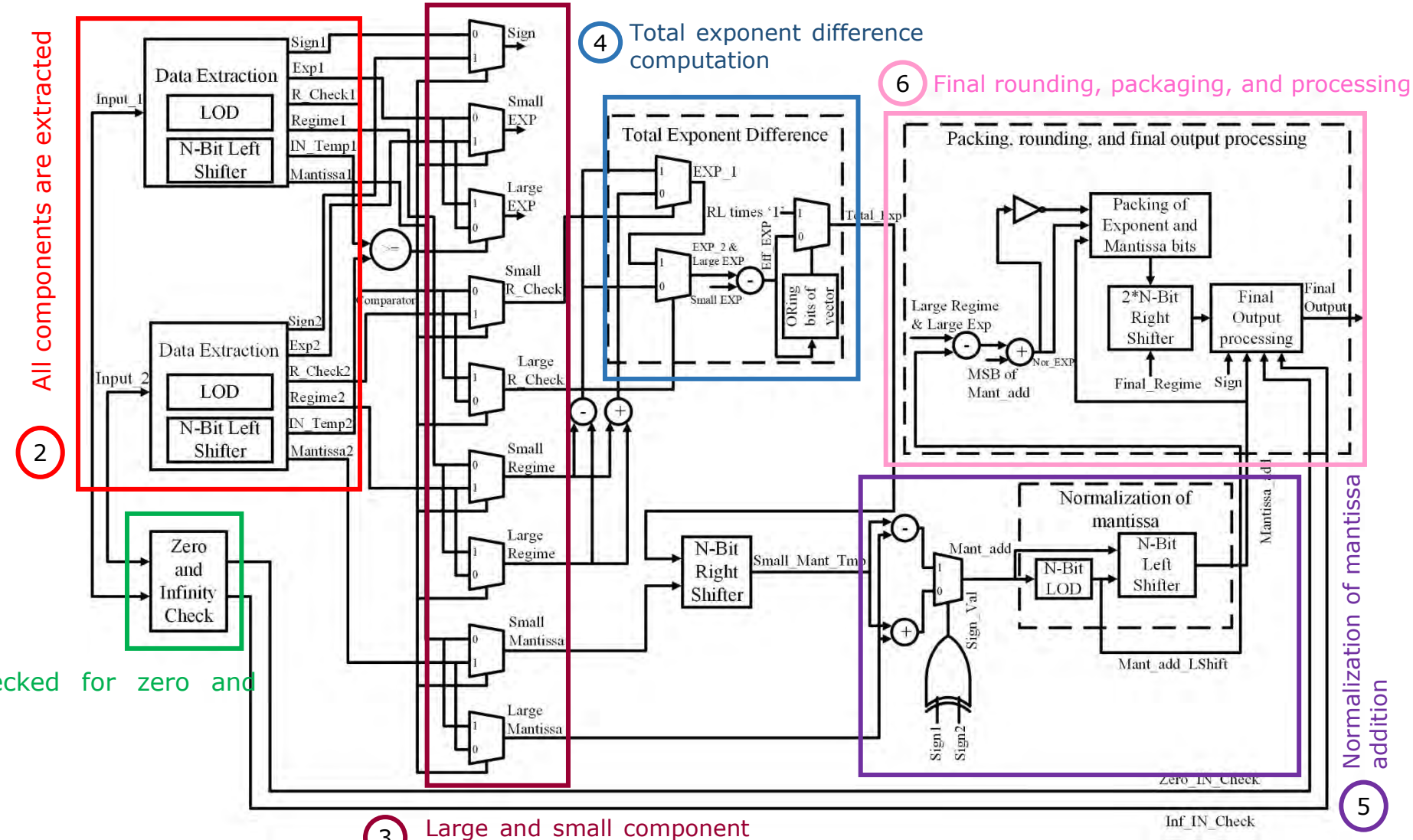
Introduction

- Posit is introduced in year 2017
- Designed for software and hardware implementations
- Its format consists of four fields: sign, regime, exponent and fraction

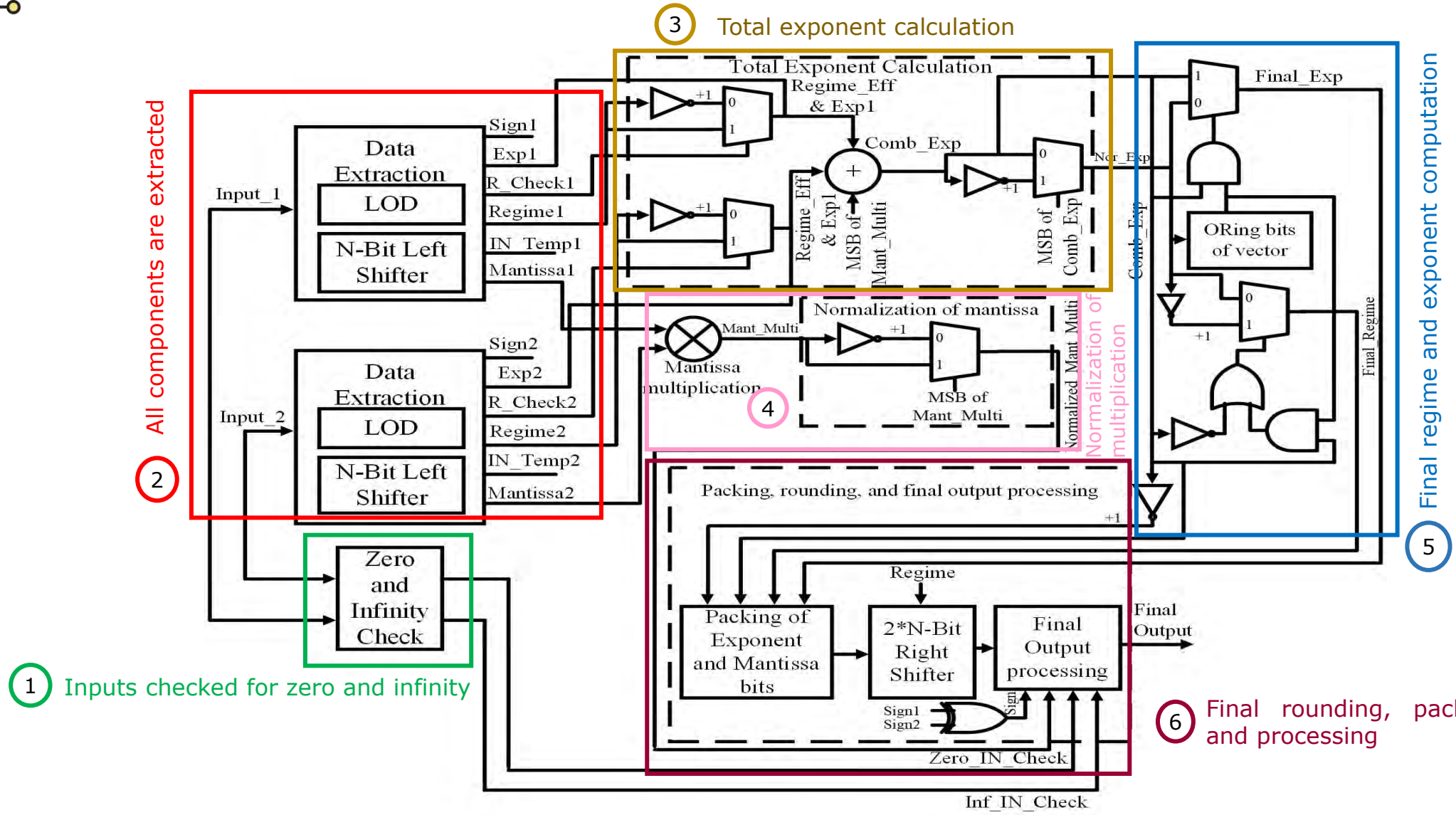


- Hardware acceleration is advantageous for performance
- Utilized in hardware accelerators

An Architecture for Posit Adder/Subtractor

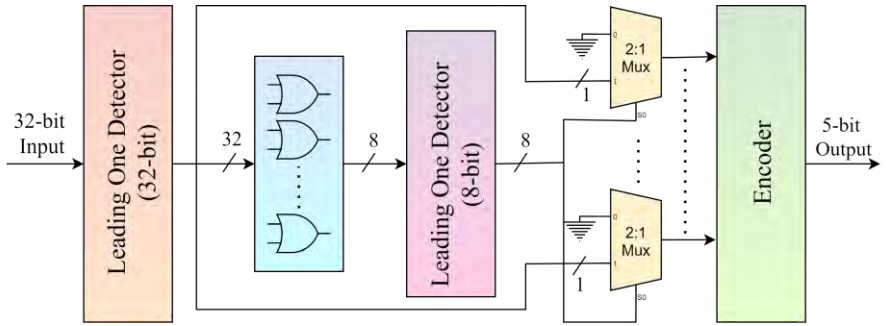


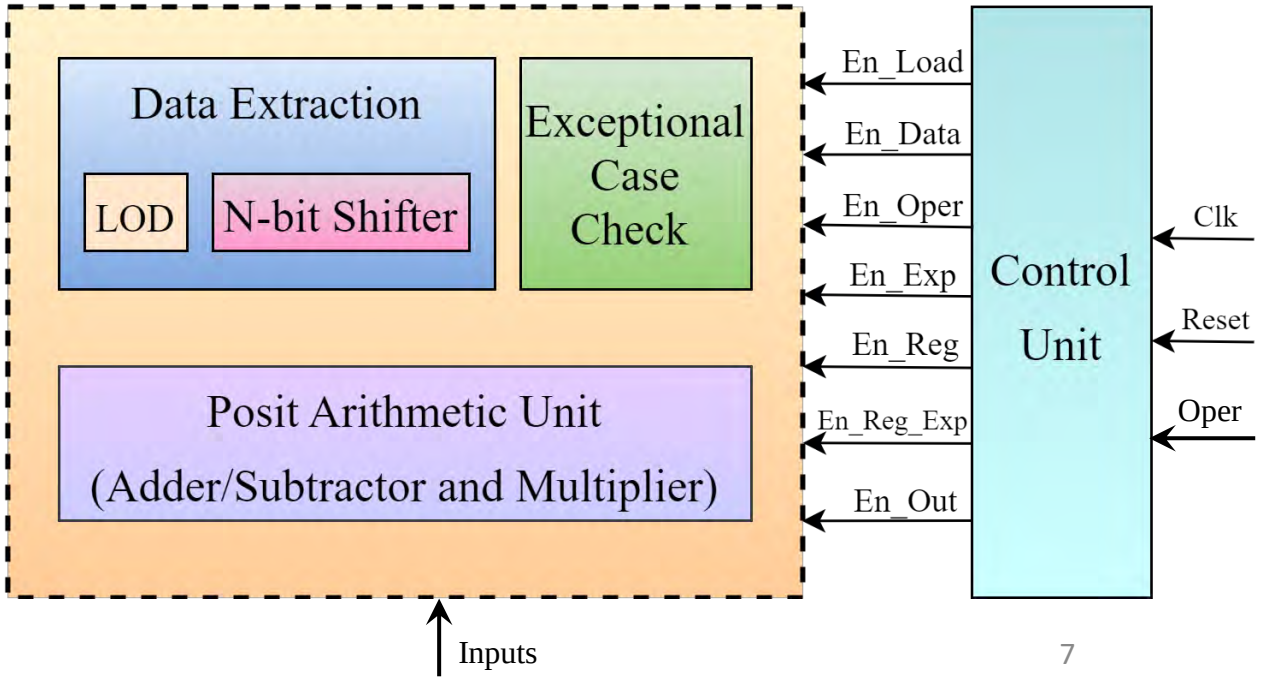
An Architecture for Posit Multiplier



Control Unit

- Enables the component that are required to be initiated
  - En_Load: Load data into the hardware accelerator
  - En_Data: Data extracted from the inputs
  - En_Oper: Arithmetic operation is performed
  - En_Exp: Compute exponent
  - En_Reg: Compute regime
  - En_Reg_Exp: Combine final regime and exponent components
  - En_Out: Final output computed





Resource Utilization

- In Virtex-7 FPGA, resource utilization

Resource utilization of 32-bit posit adder and multiplier for different values of *ES* on the Virtex-7 FPGA device

S.No.	Bit Pattern	Posit Adder		Posit Multiplier		
		LUTs	Flip-Flops	LUTs	Flip-Flops	DSPs
1.	(32,1)	1587	291	449	119	4
2.	(32,2)	1611	130	448	120	4
3.	(32,3)	1634	135	444	121	4
4.	(32,4)	1577	297	438	122	4
5.	(32,5)	1585	299	456	123	4
6.	(32,6)	1263	312	446	124	4

- In Zynq UltraScale+ FPGA, resource utilization

Resource utilization of 32-bit posit adder and multiplier for different values of *ES* on the Zynq UltraScale+ FPGA

S.No.	Bit Pattern	Posit Adder		Posit Multiplier		
		LUTs	Flip-Flops	LUTs	Flip-Flops	DSPs
1.	(32,1)	1641	291	427	119	4
2.	(32,2)	1633	230	423	120	4
3.	(32,3)	1647	235	429	121	4
4.	(32,4)	1623	297	429	122	4
5.	(32,5)	1629	299	427	123	4
6.	(32,6)	1540	312	430	124	4

Performance Comparison

Comparison of datapath delay for 32-bit posit adder and multiplier on the Virtex-7 FPGA

S.No.	Bit Pattern	Posit Adder		Posit Multiplier	
		[JAIS19]	Proposed	[JAIS19]	Proposed
1.	(32,1)	19.150	7.534	19.076	9.310
2.	(32,2)	19.984	6.896	18.921	9.310
3.	(32,3)	19.752	6.389	19.203	8.453

- Datapath delay is reduced
  - Adder → 64.64%
  - Multiplier → 52.66%

Comparison of area-delay product for 32-bit posit adder and multiplier on the Virtex-7 FPGA

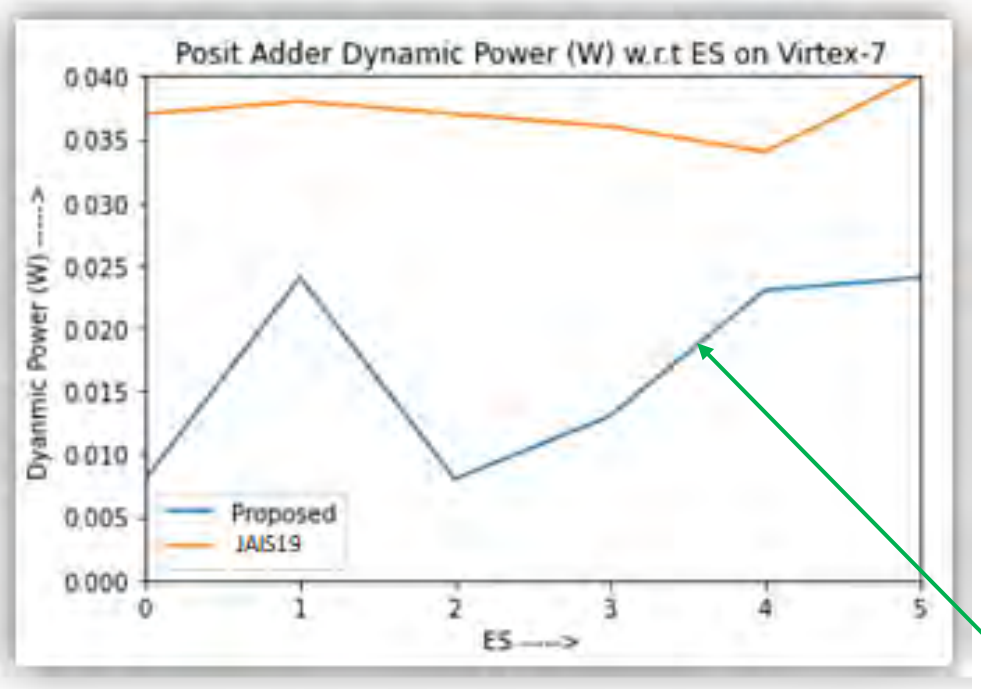
S.No.	Bit Pattern	Posit Adder		Posit Multiplier	
		[JAIS19]	Proposed	[JAIS19]	Proposed
1.	(32,1)	23190.65	11956.45	12742.77	4180.19
2.	(32,2)	25480.00	11109.46	12866.28	4170.88
3.	(32,3)	22155.00	10439.62	13826.20	3753.12

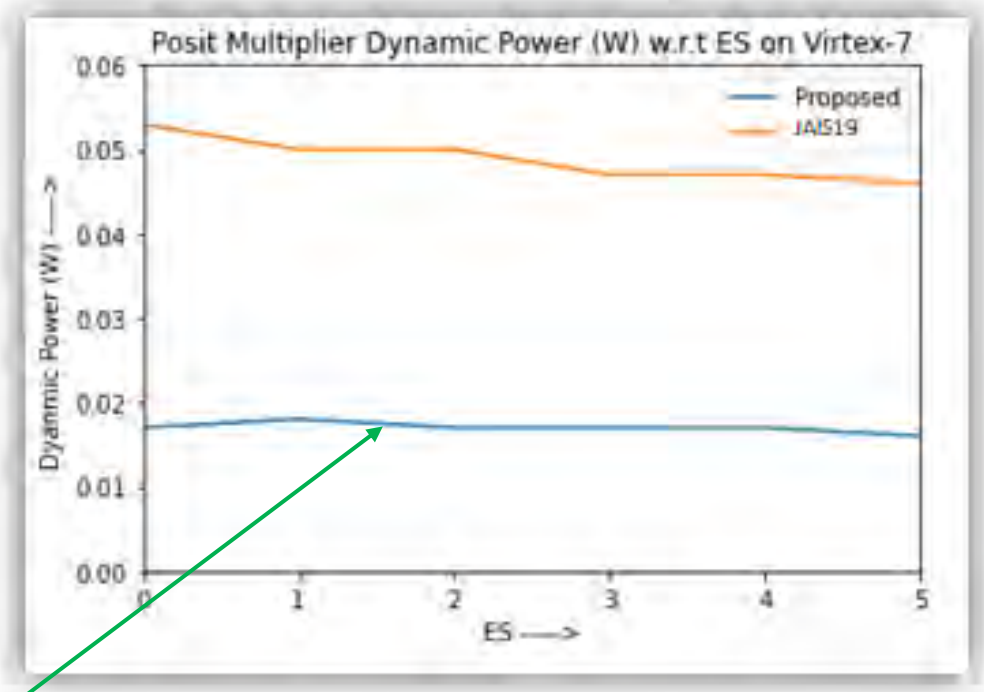
- Area-delay product is reduced
  - Adder → 52.69%
  - Multiplier → 69.30%

[JAIS19] Jaiswal, Manish Kumar, and Hayden K-H. So. "Pacogen: A hardware posit arithmetic core generator." *IEEE Access* 7 (2019): 74586-74601.

Dynamic Power Comparison

- Lower dynamic power than the existing architecture





Lower dynamic power

[JAIS19] Manish Kumar, and Hayden K-H. So. "Pacogen: A hardware posit arithmetic core generator." *IEEE Access* 7 (2019): 74586-74601.

Conclusion

- Posit is an alternative of floating-point
- Proposed hardware architectures and control unit for the Posit arithmetic
- Implementation on the Xilinx Virtex-7 and Zynq UltraScale+ devices
  - For a range of *ES* values
- Resource utilization
  - Adder → 0.60%, Multiplier → 0.40%
- Reduced
  - Datapath delay
    - Adder → 64.64%, Multiplier → 52.66%
  - Area-delay product
    - Adder → 52.69%, Multiplier → 69.30%
- Improved (reduced) dynamic power

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Thank You !